REMARKS

Reconsideration and further examination of the present application is respectfully requested. The Office Action has rejected claims 1-15 and 37-50. Applicant thanks the Examiner for accepting the referenced application's drawings.

Applicants amended claims 1-4, 6, 8, 10-13, 37, and 42-50 to clarify limitations already present in the claims, thus added no new matter.

Objections to the Claims

Examiner has objected to claims 44 and 47 because of the following informalities: The phrase "said first clock cycle" in lines 6-7 should be changed to "a first clock cycle" as there is no first clock cycle earlier in the claim.

Applicant amended claim 44 and 47 so that "said first clock cycle" now reads "a first clock cycle."

35 U.S.C. § 103

Claims 1-14 and 47-49 have been rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent Application Pub. No. 2002/0176449 to Trippe ("Trippe") in view of U.S. Patent No. 5,081,654 to Stephenson, Jr., et al. ("Stephenson").

Claims 37-46 and 50 have been rejected under 35 U.S.C. 103 (a) as being unpatentable over Trippe in view of Stephenson and in further view of U.S. Patent No. 5,465,345 to Blanc et al. ("Blanc").

Claim 15 has been rejected under 35 U.S.C. 103 (a) as being unpatentable over Trippe in view of Stephenson and in further view of U.S. Patent No.6,970,563 to Risling ("Risling").

Claim 1

Claim 1 requires storing a current at least two bytes of bit-synchronous High-level Data Link Control data in a shift register. Claim 1 also requires processing in parallel said current at least two bytes within said shift register so as to detect a start-of-frame sequence within said current at least two bytes in said shift register during a first clock cycle with a plurality of comparators coupled with said shift register, wherein each comparator is coupled with said shift register to parallel process a unique combination of eight successive bits within said shift register. Moreover, claim 1 requires processing in parallel said current at least two bytes within said shift register so as to detect an end-of frame sequence within said current at least two bytes in said shift register during at least one subsequent clock cycle with said plurality of comparators coupled with said shift register.

Trippe and Stephenson fail to describe the above limitations of claim 1 individually or in combination. Specifically, Trippe describes an HDLC frame receiver that processes eight HDLC frame bits in parallel[1]. (Trippe , para. 37). As shown in Figure 3 and described in paragraphs 43 and 44, a receiver processes a group of bits in groups of eight bits. Because the receiver only processes eight bits at a time, a flag may be spread over multiple bit groups. Furthermore, Trippe describes the need of a bit accumulator because the receiver only processes eight bits at a time and a flag my straddle multiple bit groups. (Trippe, para. 43) Thus, the need to temporarily store the first set of eight bits in a bit accumulator until a second set of eight bits is processed. This also indicates the receiver of Trippe takes more than one clock to detect a flag

[1] Trippe describes "the framer 200 may be configured to simultaneously process 2n (e.g., 2, 4, 8, 16, 32 . . .) or some other number of bits," but not a receiver simultaneously processing more than 8 bits. (para. 26, emphasis added). A framer is not equivalent to a receiver because they perform different functions and

within two bytes (i.e. 16 bits).

Thus, Trippe fails to describe storing two bytes of HDLC data in a shift register and processing two bytes of data within a shift register with a plurality of comparators coupled with a shift register as required by claim 1. Furthermore, Trippe fails to describe processing in parallel two bytes to detect a start-of frame sequence during a first clock cycle and to detect an end-of frame sequence during at least one subsequent clock cycle.

Stephenson describes an implementation of a parallel synchronization circuit designed to find the adjacent framing bytes of a three channel SONET standard in a bit stream converted to eight bits. Stephenson describes using a serial to parallel converter to create a parallel data of four bits in a first clock. Then, Stephenson describes converting the 4 bit data to 8 bit parallel data at a second clock cycle by means of three more latches. (Stephenson, Figure 3 and col. 5, ll. 55-66). This eight bits data word is then clocked in and out of three sequential latches. "Each subsequent data word causes the previous data word to be shifted to the next latch." (col. 6, ll. 15-18). As the data word is shift out of the three sequential latches the eight bits are presented to a combination of detectors to deframe the SONET bit stream. (col. 6, ll. 24-36).

Thus, Stephenson fails to describe storing two bytes of HDLC data in a shift register and processing two bytes of data within a shift register with a plurality of comparators coupled with a shift register as required by claim 1. Furthermore, Stephenson fails to describe processing two bytes to detect a start-of frame sequence during a first clock cycle and to detect an end-of frame sequence during at least one subsequent clock cycle.

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have different operating constraints. Therefore, describing a framer having the ability to simultaneously process more than eight bits is not equivalent to a receiver processing more than eight bits.

Therefore, the combination describes a serial bit stream converted to a parallel eight bit stream according to Stephenson taking multiple clock cycles. The eight bits are then clocked out of an eight bit latch to a receiver according to Trippe. As discussed above, Trippe describes a receiver that processes eight bits at a time necessitating the need for an accumulator. Moreover, the combination requires more than a first clock cycle to detect a flag within two bytes of data.

Because the above limitations of claim 1 are not described or suggest by the combination, the combination fails to render claim 1 obvious.

Claims 2-4

Applicants respectfully submit that claims 2-4 are dependent directly or indirectly on claim 1, thus include the same limitations as claim 1. As such, claims 2-4 are allowable for at least the same reasons as claim 1.

Claims 44 and 47

Claims 44 and 47 contain limitations similar to the limitations of claim 1 discussed above. Therefore, claims 44 and 47 are allowable for at least the reasons discussed above.

Claims 45 and 46

Applicants respectfully submit that claims 45 and 46 are dependent directly or indirectly on claim 44, thus include the same limitations as claim 44. As such, claims 45 and 46 are allowable for at least the same reasons as claim 44.

Claims 48-50

Applicants respectfully submit that claims 48-50 are dependent directly or indirectly on claim 47, thus include the same limitations as claim 47. As such, claims 48-50 are allowable for at least the same reasons as claim 47.

Claim 6

Claim 6 requires processing in parallel said current at least two bytes within said shift register so as to detect valid payload data bits within said current at least two bytes using a plurality of comparators coupled with said shift register to search for a specified sequence of bits stored within said at least two bytes during a first clock cycle, wherein each comparator is coupled with said shift register so as to parallel process a unique combination of eight successive bits contained within said shift register.

As discussed above, the combination describes a receiver that processes eight bits at a time. Moreover, the receiver requires more than a first clock cycle to detect a flag in two bytes of data. Furthermore, the combination fails describe or suggest the use of a plurality of comparators to detect valid payload data bits with in two bytes as required by claim 6. Therefore the combination fails to render claim 6 obvious.

Claims 8-13 and 15

Applicants respectfully submit that claims 8-13 and 15 are dependent directly or indirectly on claim 6, thus include the same limitations as claim 6. As such, claims 8-13 and 15 are allowable for at least the same reasons as claim 6.

Claim 37

Claim 47 contains limitations similar to the limitations of claim 6 discussed above. Therefore, claim 47 are allowable for at least the reasons discussed above.

Claims 38-46

Applicants respectfully submit that claims 38-46 are dependent directly or indirectly on claim 37, thus include the same limitations as claim 37. As such, claims 38-46 are allowable for at least the same reasons as claim 37.

Conclusion

In view of the foregoing remarks and amendments, it is respectfully submitted that the present application is in condition for allowance.

Invitation for a telephone interview

The Examiner is invited to call the undersigned at 408-720-8300 if there remains any issue with allowance of this case.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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